

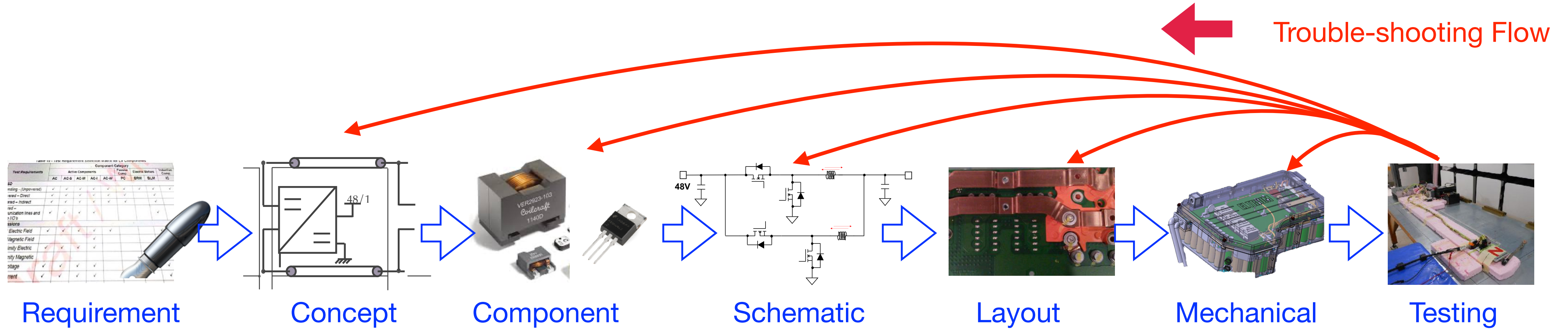
Essential EMC Training for Design Engineers

Dr. Min Zhang

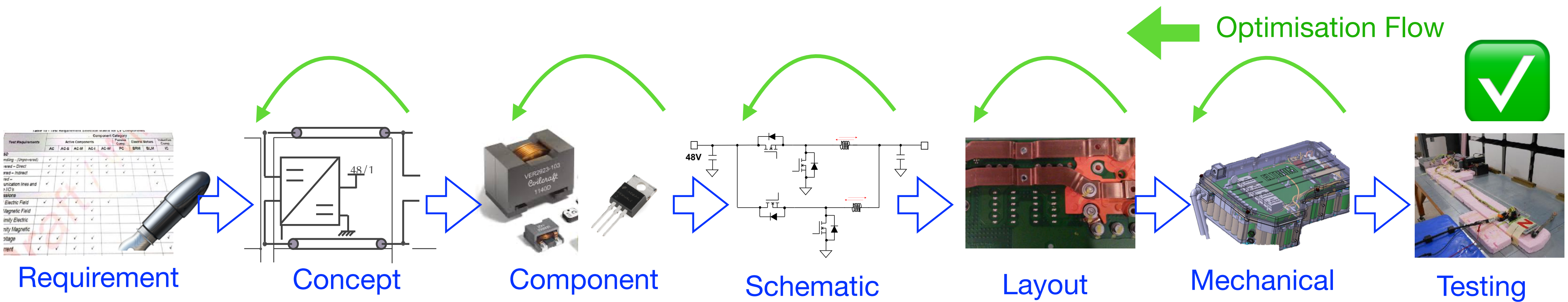
A Mach One Design Training Material



Our approach



Design Flow



Design Flow

Training Programme Pyramid Structure

Filter Design

SMPS & Motors

PCB Design

Digital & Analog Design

High frequency measurement & troubleshooting

TOP Level

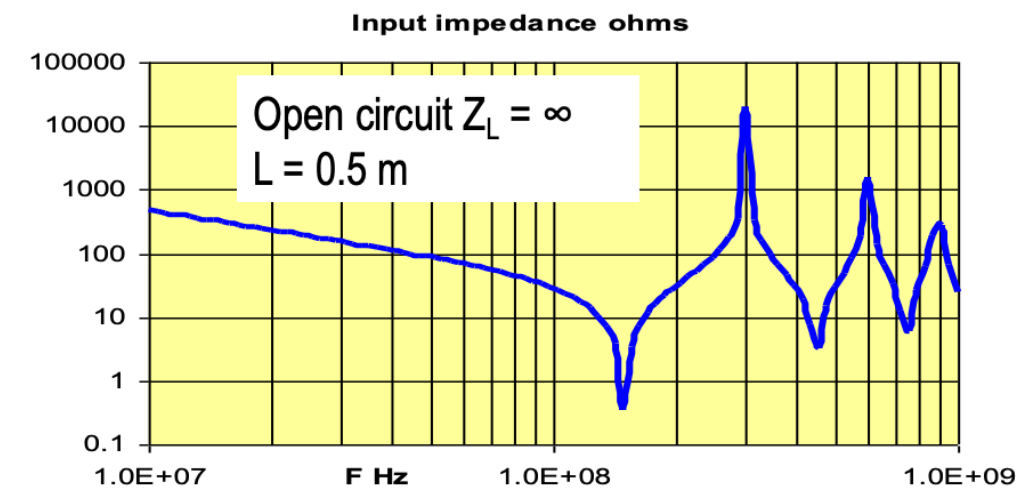
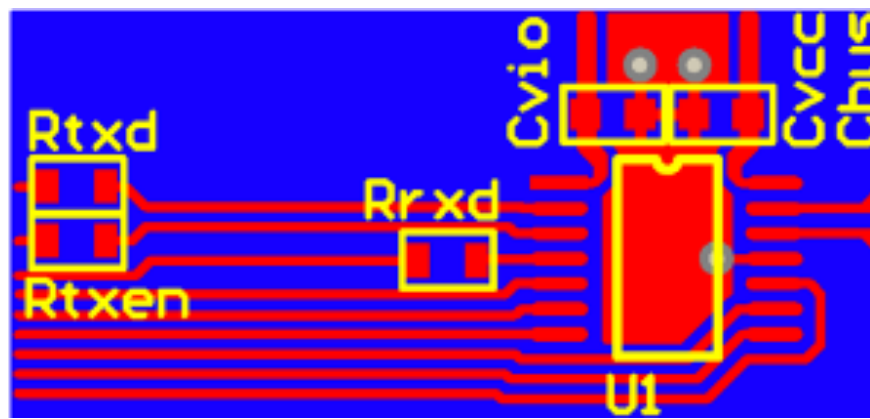
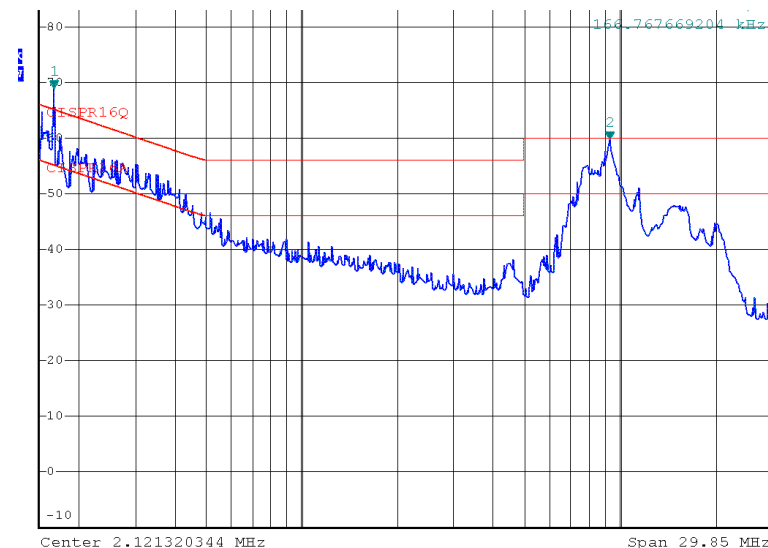
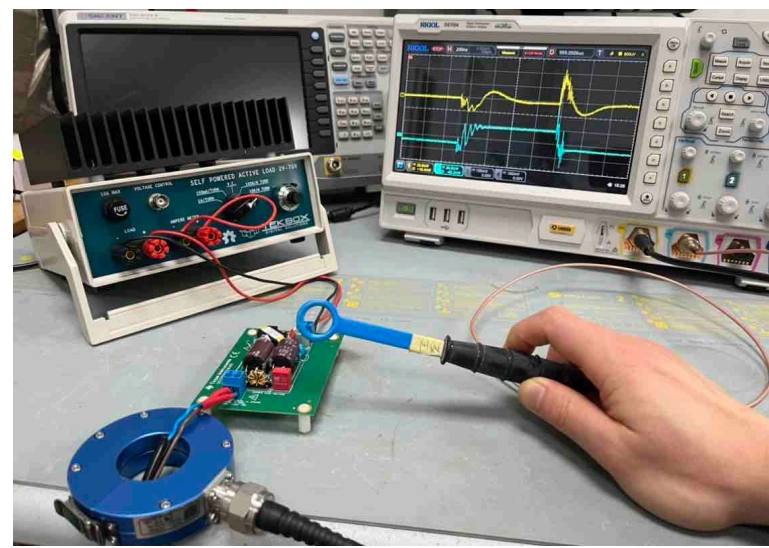
Filtering (Ferrite)

Shielding

Grounding

Cables & Connectors

Medium Level



Fundamental

Module 1

Module 2

Module 3

Module 4

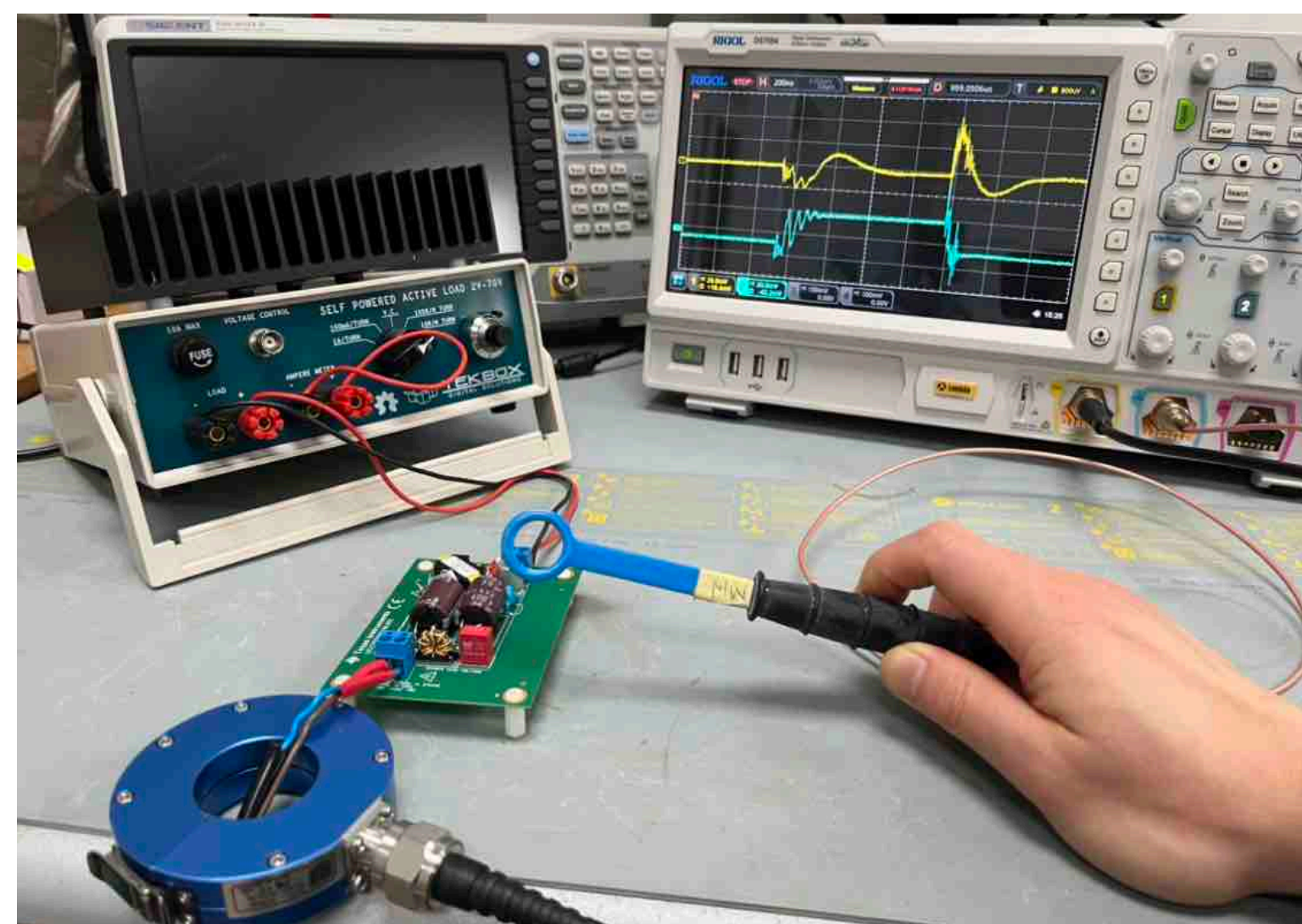
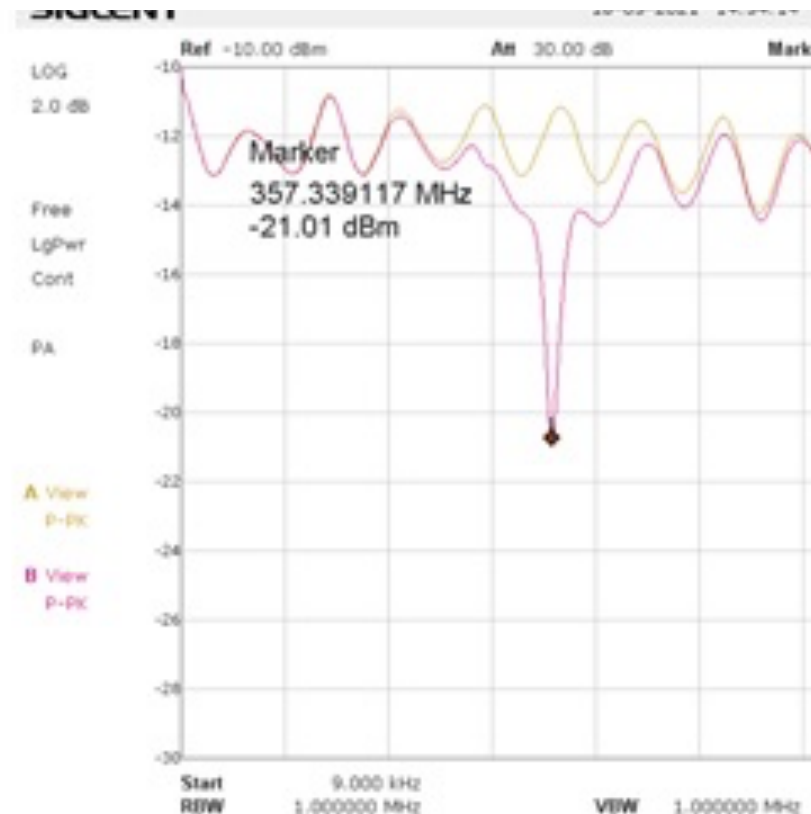
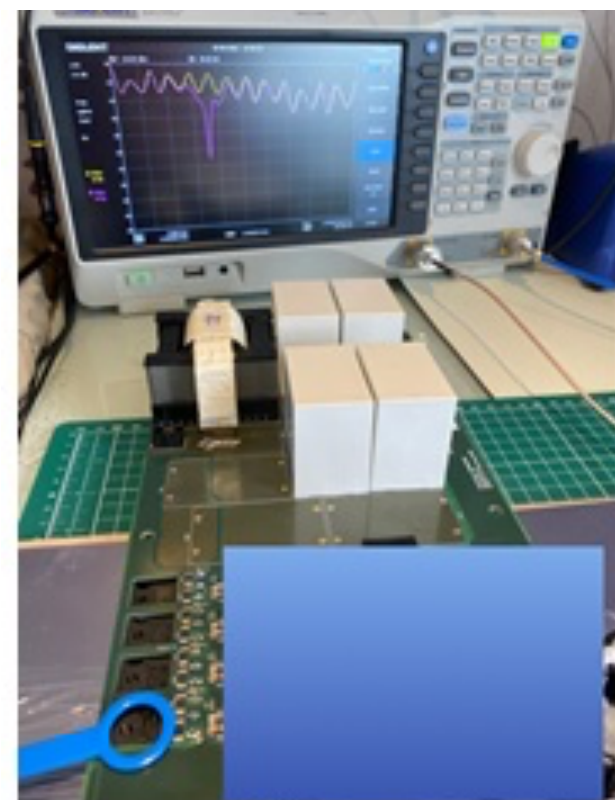
Design for EMC Course Objectives - 3 day



- Introduction to EMI, EMC & SIPI
- The purpose of this course - introducing the first principles and the tools
- Understand EMC design principles for PCB level; grounds, trace coupling, multi-layer PCB
- Understand EMC design principles for cables and connections
- Understand EMC design principles for shielding
- Understand EMC design principles for filtering
- Understand EMC design techniques for switched converters
- Understand EMC design principles for digital and analogue circuits

High-Frequency Measurement and Troubleshooting Course Objectives - 2 day

- Understand the first principles of high-frequency measurement.
- Avoid pitfalls of high-frequency high-speed measurement.
- Understand direct contact measurement techniques and circuit capacitive loading phenomena.
- Understand magnetic-field loops, theory, and applications.
- Learn how to use RF current probes, theory, and applications, including advanced usages.
- Master advanced troubleshooting techniques, including locating resonance structures and ESD troubleshooting.



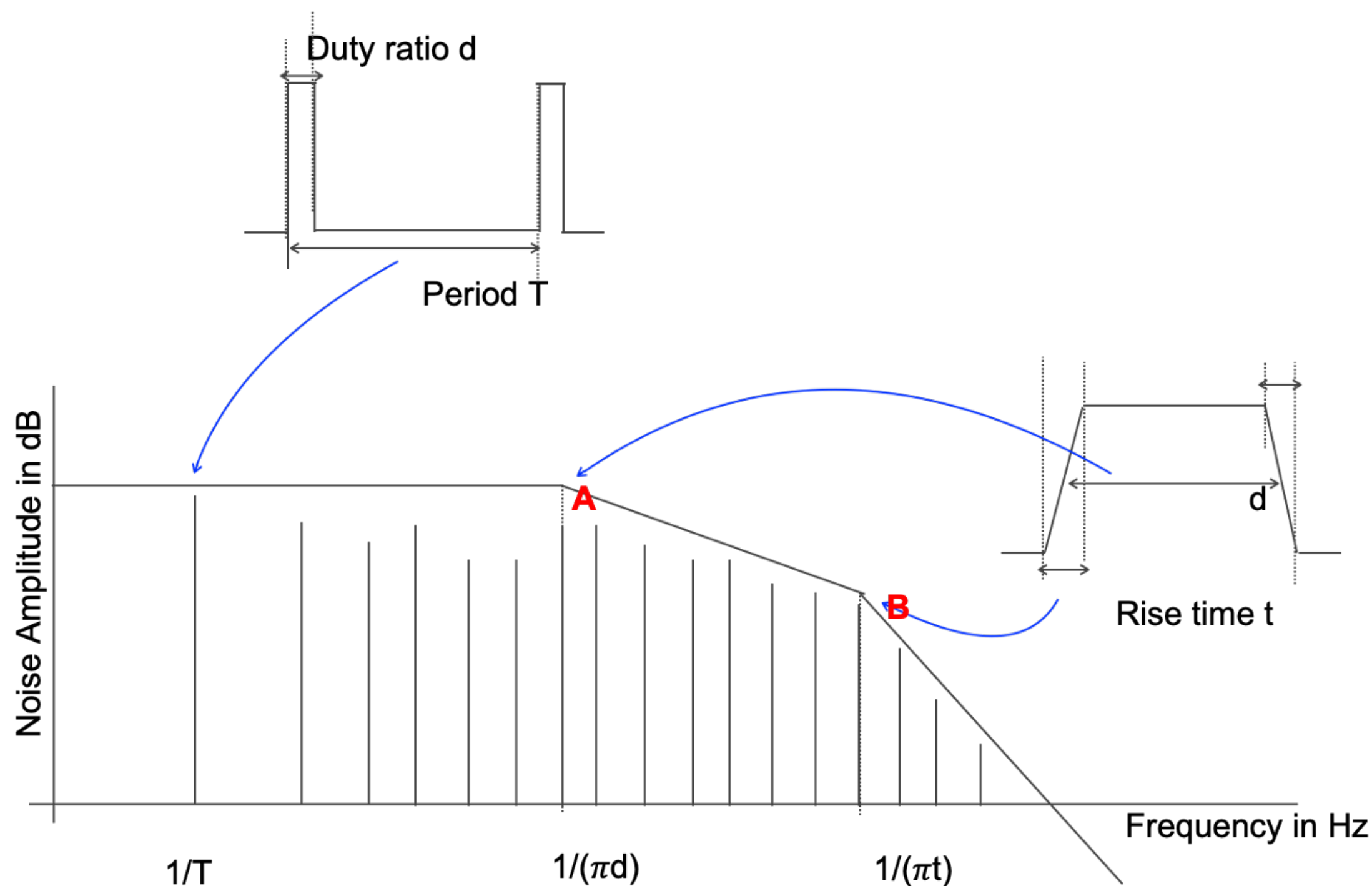
Sample Pages

Fundamentals - Module 1

Suited for engineers of all levels, including mechanical engineers, system engineers and junior-level engineers.

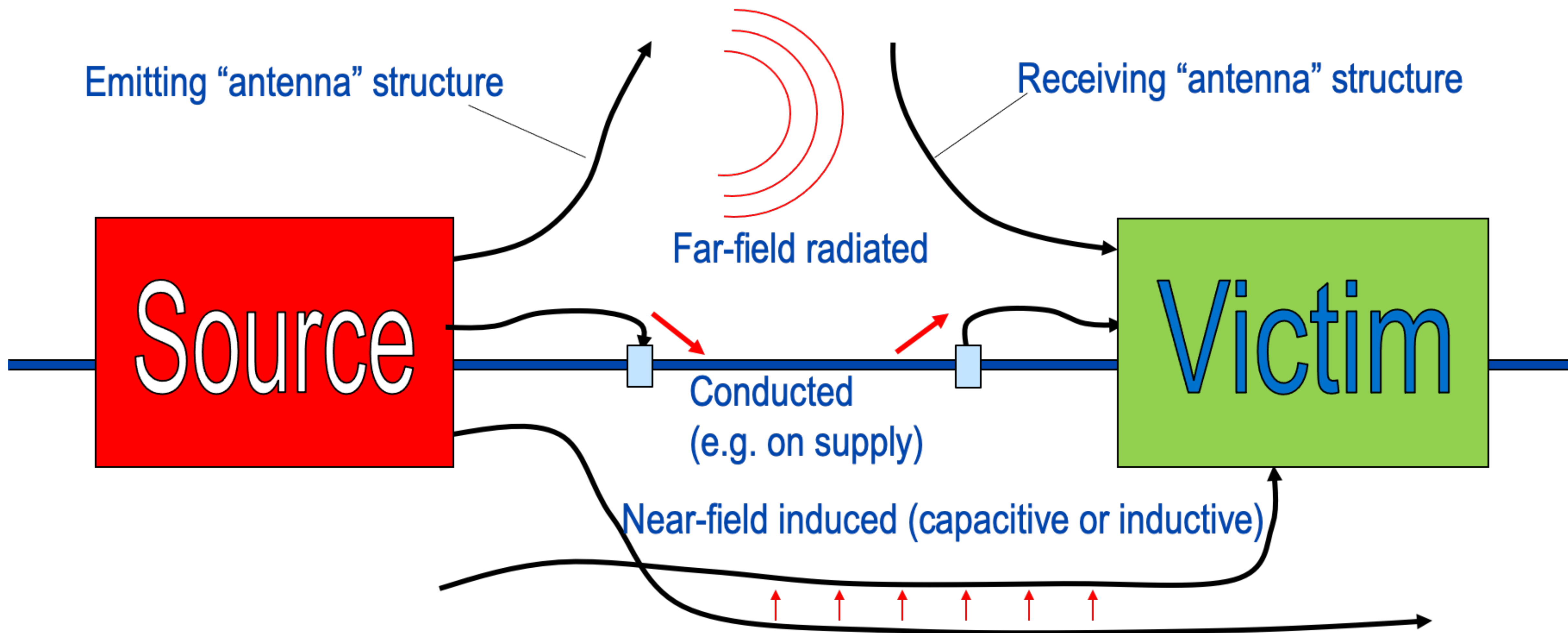
With questions designed to help engineers understand the concepts introduced in this sector. See an example on the next slide.

Envelope of spectrum of a trapezoidal pulse

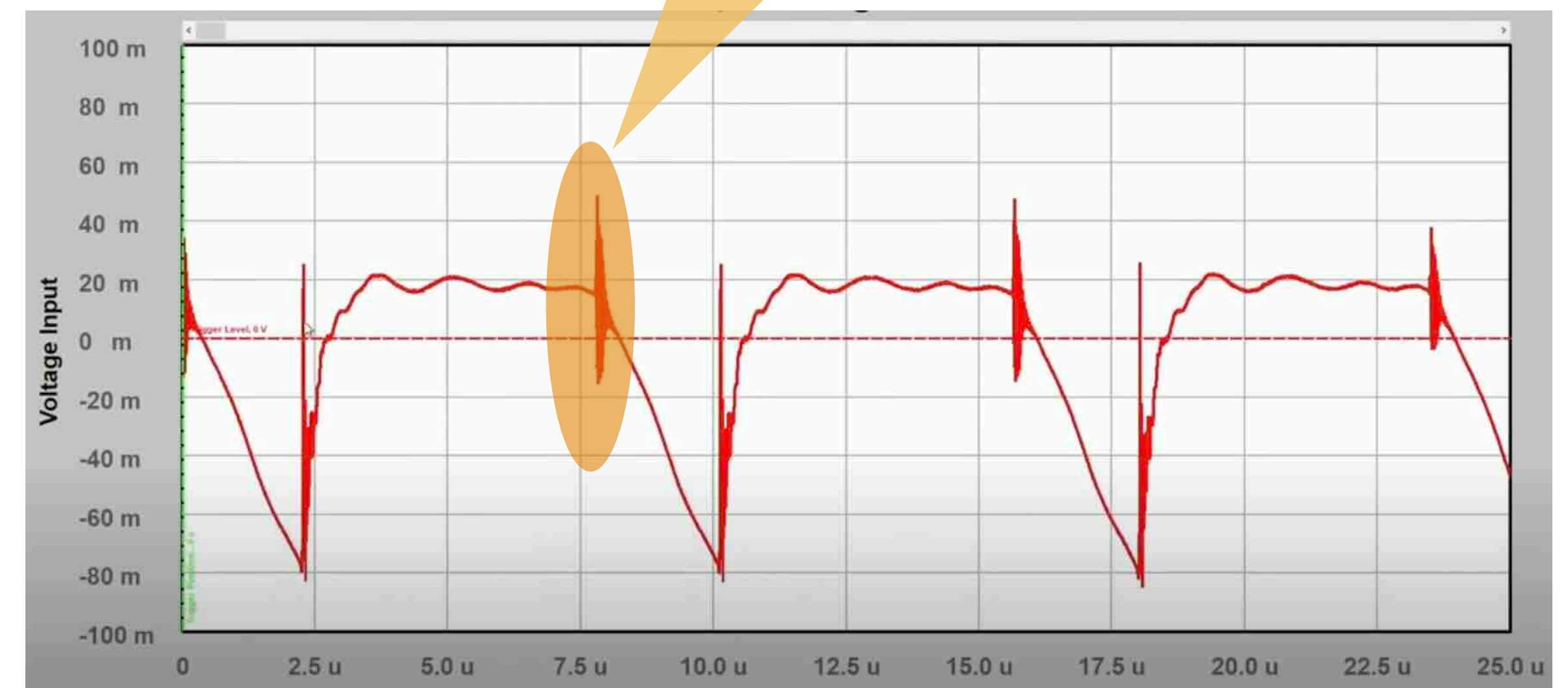
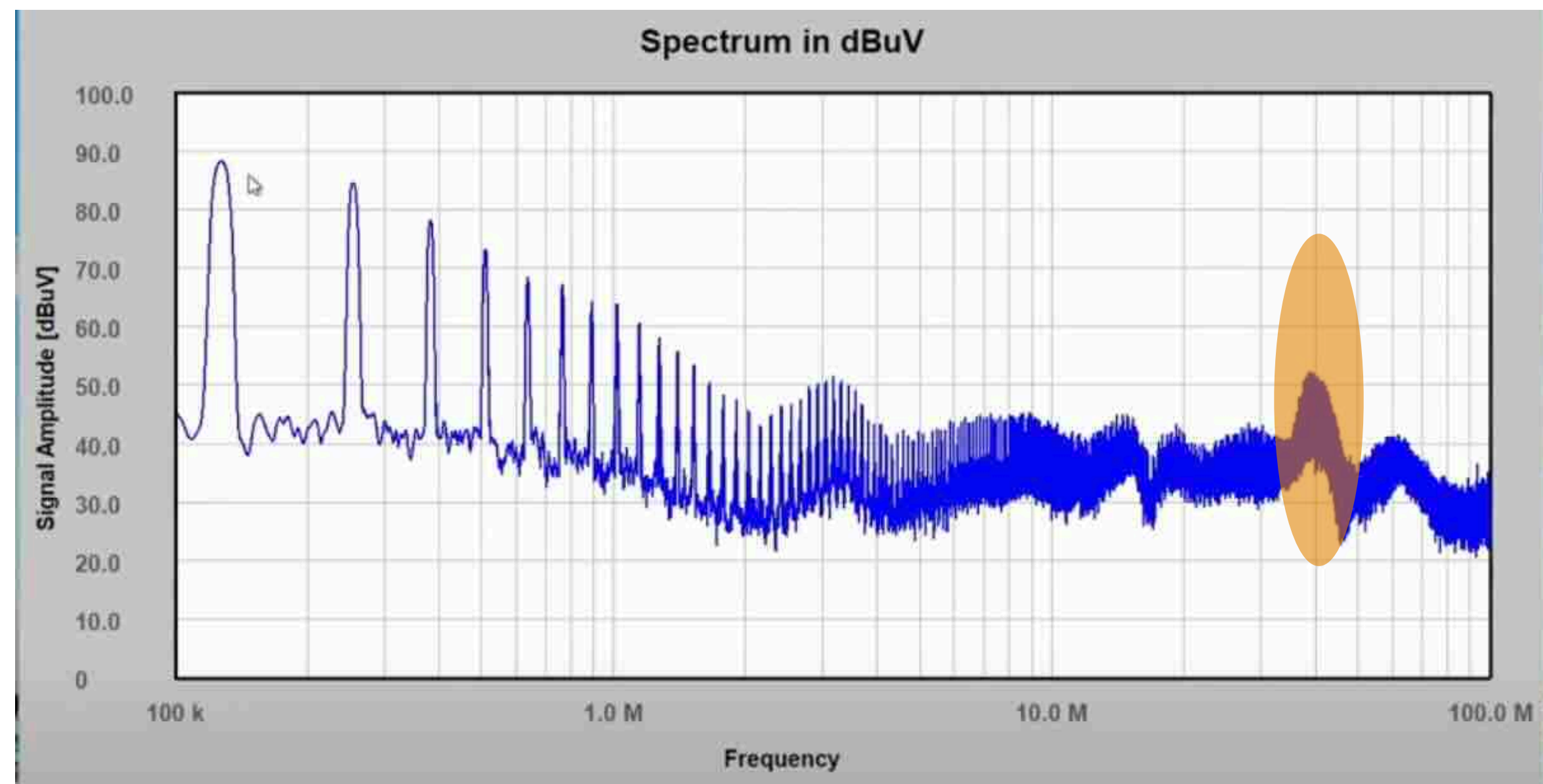
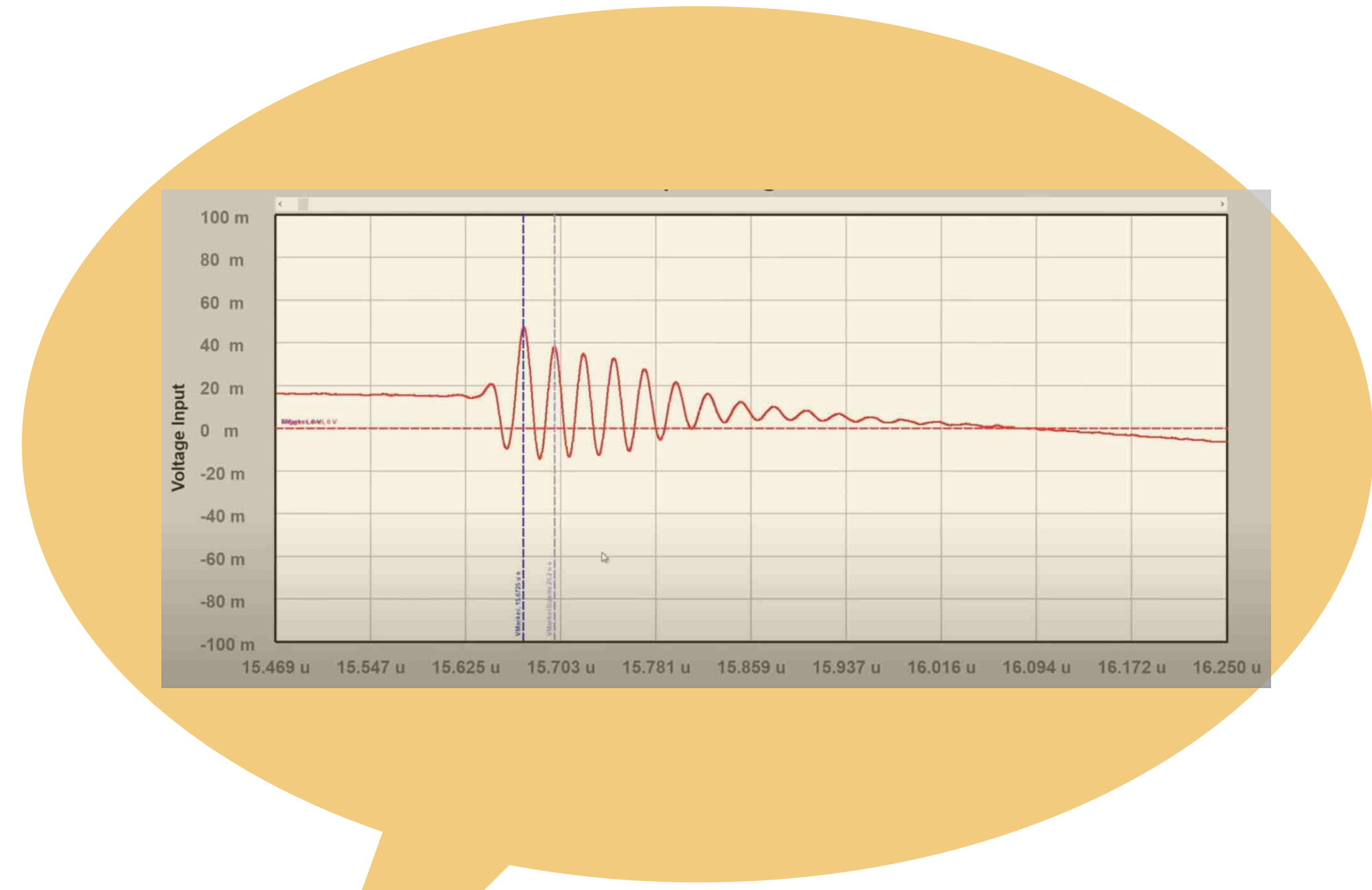


- The Decibel (dB) & using the dB
- Time versus Frequency: Trapezoidal Wave
- Broadband and Narrowband Noise
- Time vs Frequency Analysis
- Coupling Mechanisms
- Near and far fields
- Understanding Parasitics

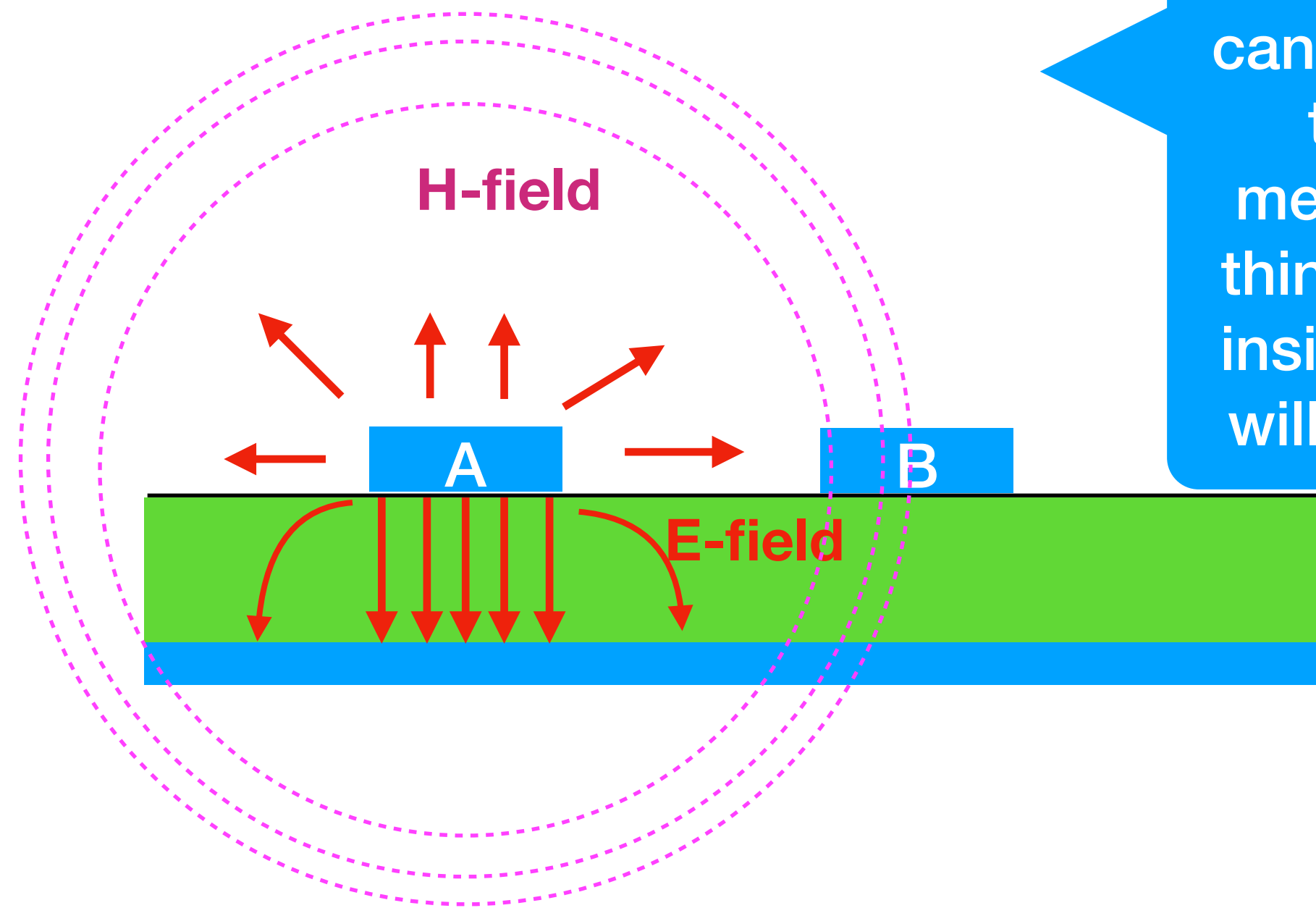
Coupling Mechanisms



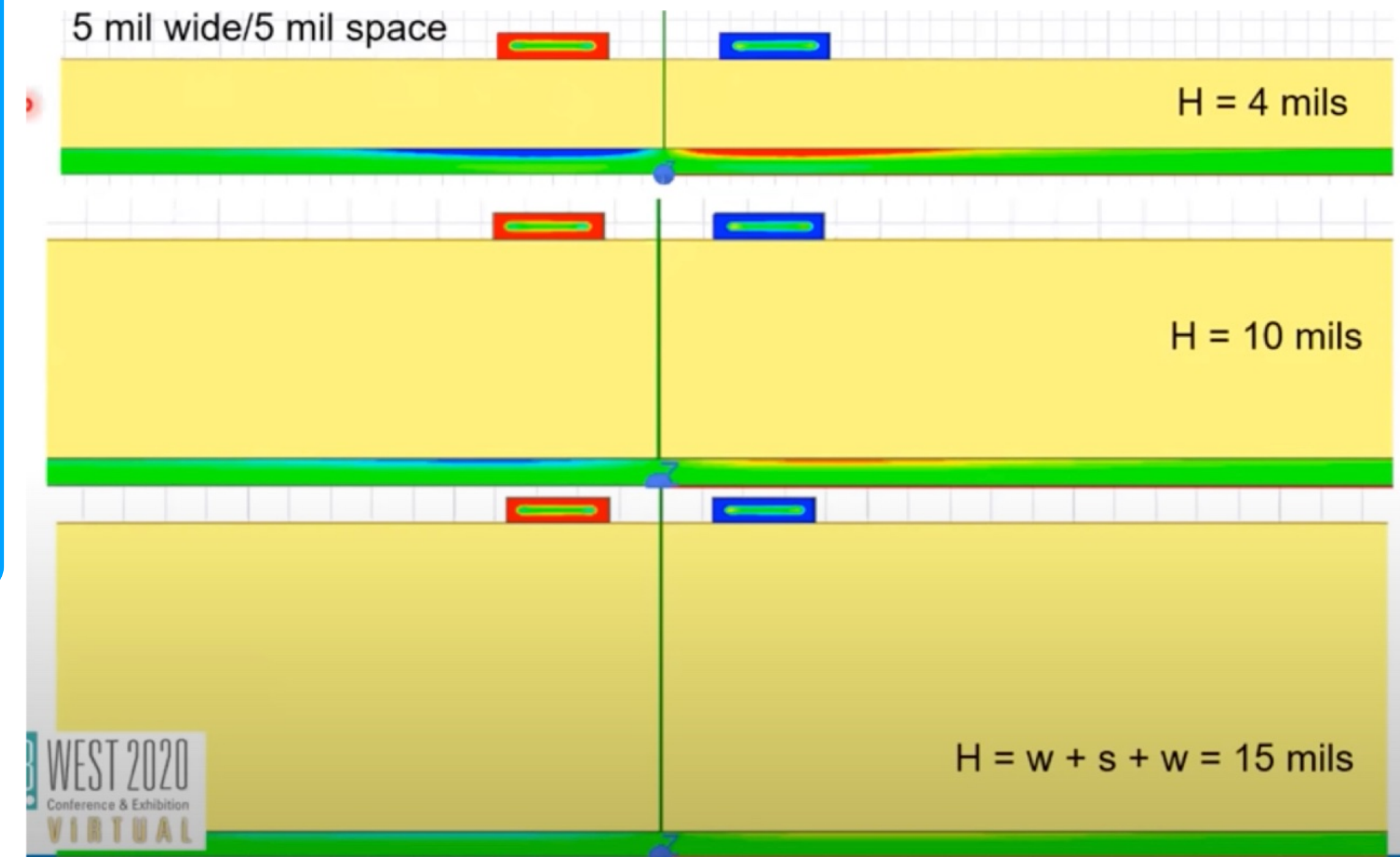
Time vs Frequency Domain



Coupling



Again, only when we understand that the field is in the space can we understand the coupling mechanism. If we think current flows inside the wire, we will never get this.

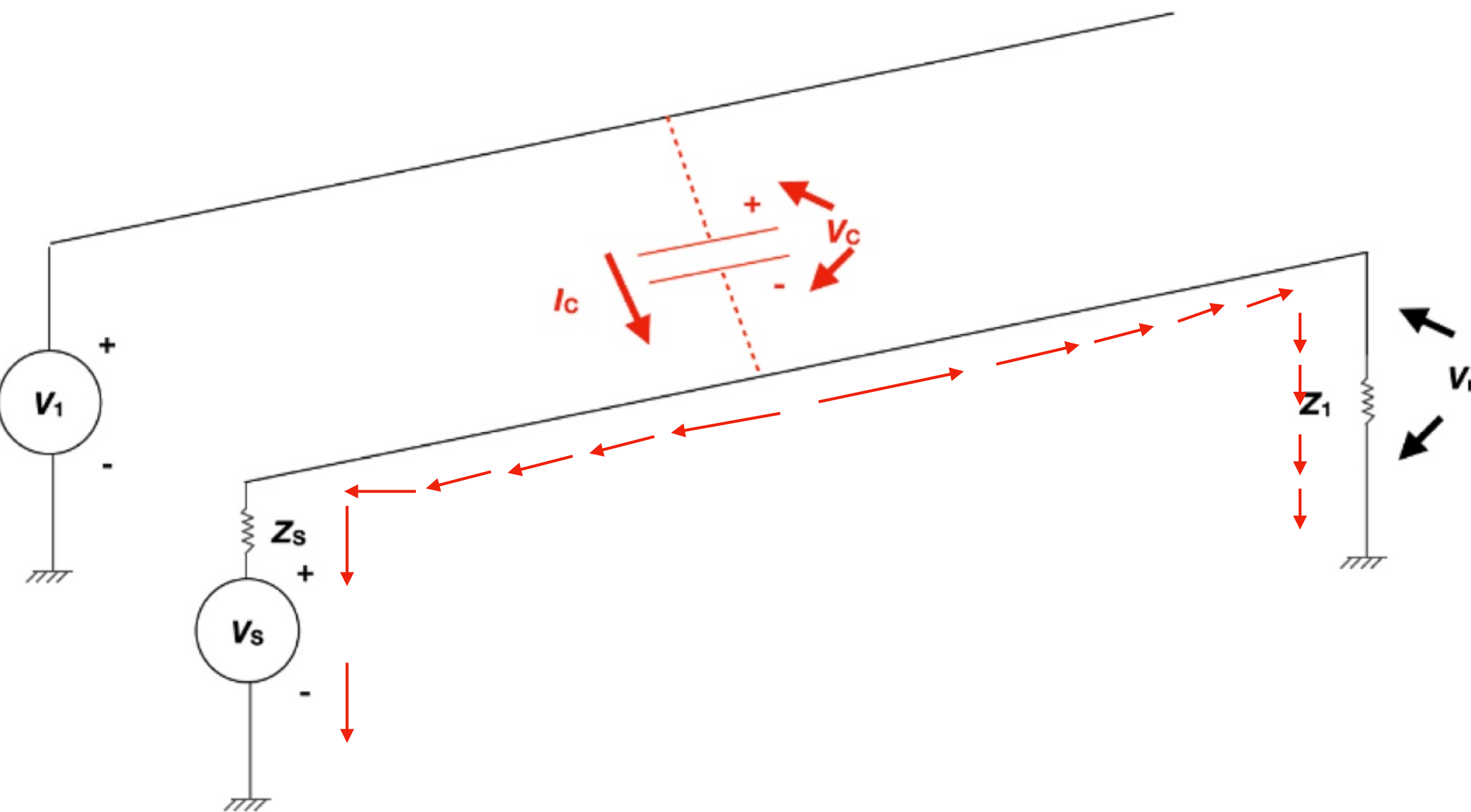


Even true differential signal pairs use a common return path. It is **NOT** true that the return current of one signal line is carried by another line. - it depends

Source: What every PCB Designer Should know - Return Current Path (with Eric Bogatin) <https://www.youtube.com/watch?v=icRzEZF3eZo>

Crosstalk, unwanted signals on other lines unintendedly - SIPI
Interference - EMC
Common mode coupling path - EMC

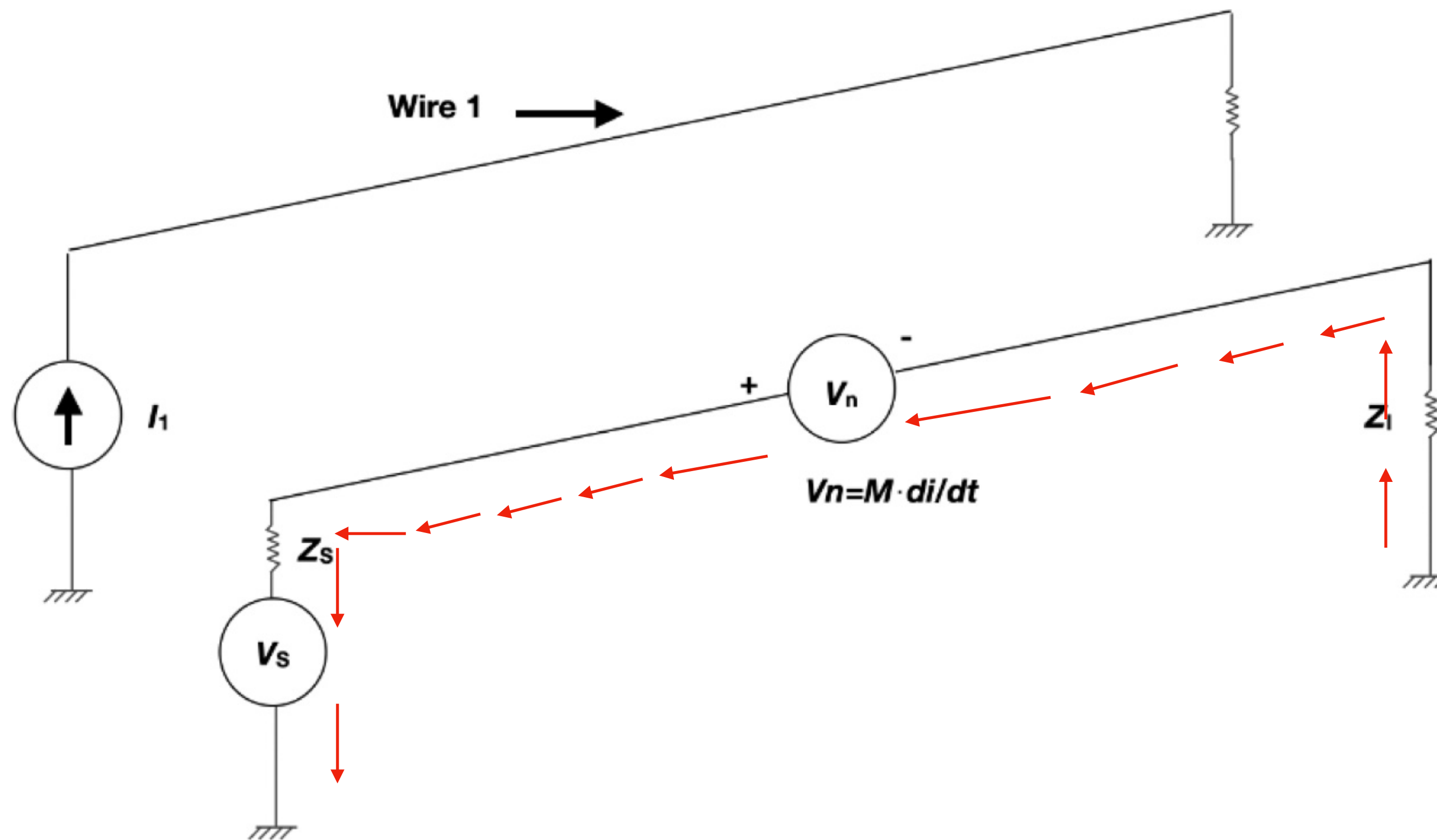
Capacitive Coupling - E-field Coupling



- Two conductors represent two parallel run wires, traces over a PCB, etc.
- Ignoring the inductance effect in this example.
- V_1 represents the noise source.
- What is the induced interference voltage on Z_l ?

$$V_n = C \frac{dV_1}{dt} (Z_s || Z_l)$$

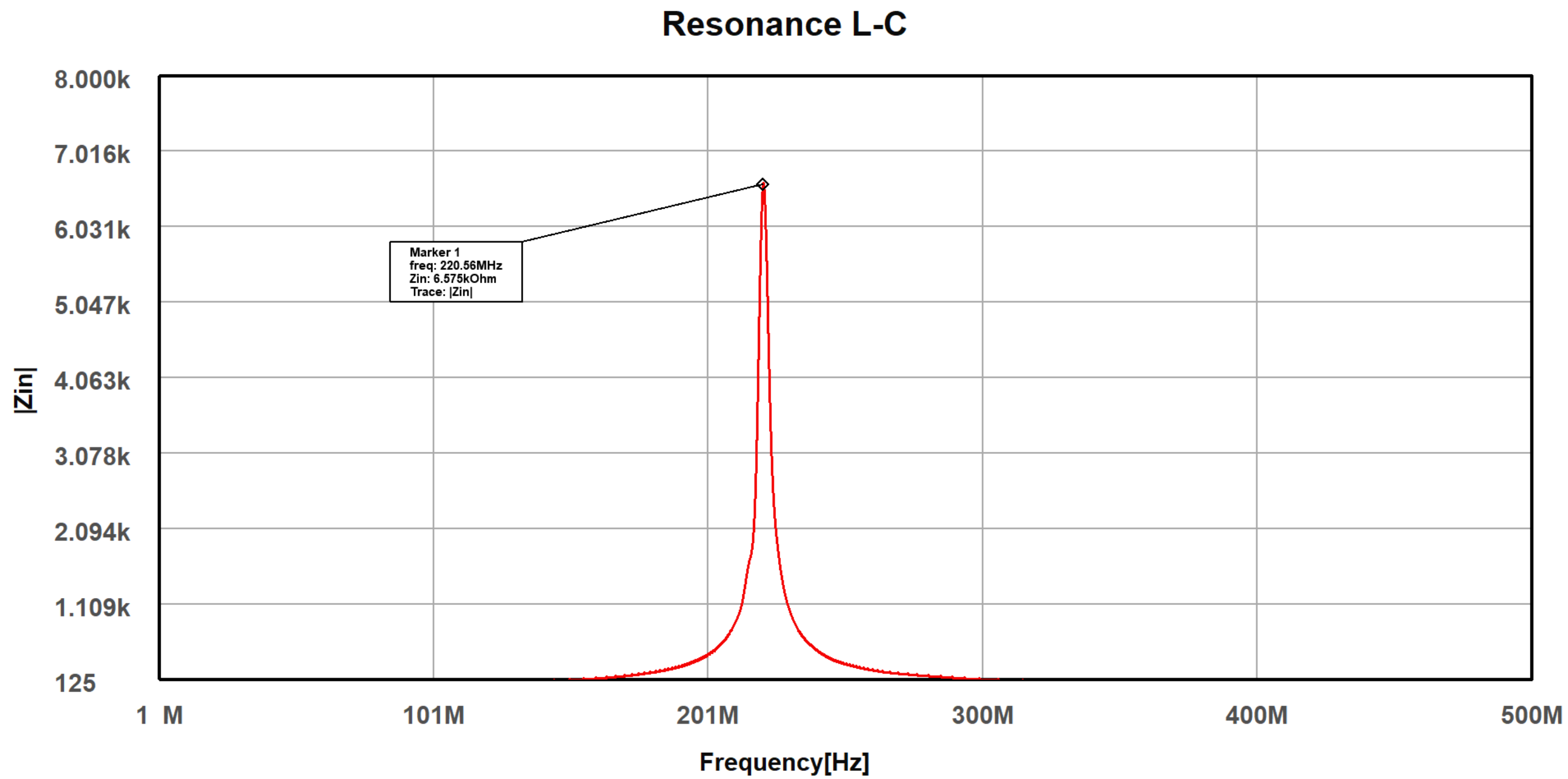
Inductive Coupling - H-field Coupling



- Two conductors represent two parallel run wires, traces over a PCB, etc.
- Ignoring the inductance effect in this example.
- I_1 represents the noise source, in this case, it is a current source.
- What is the induced interference voltage on Z_i ?

$$V_l = M \frac{dI_1}{dt} \frac{Z_l}{Z_s + Z_l}$$

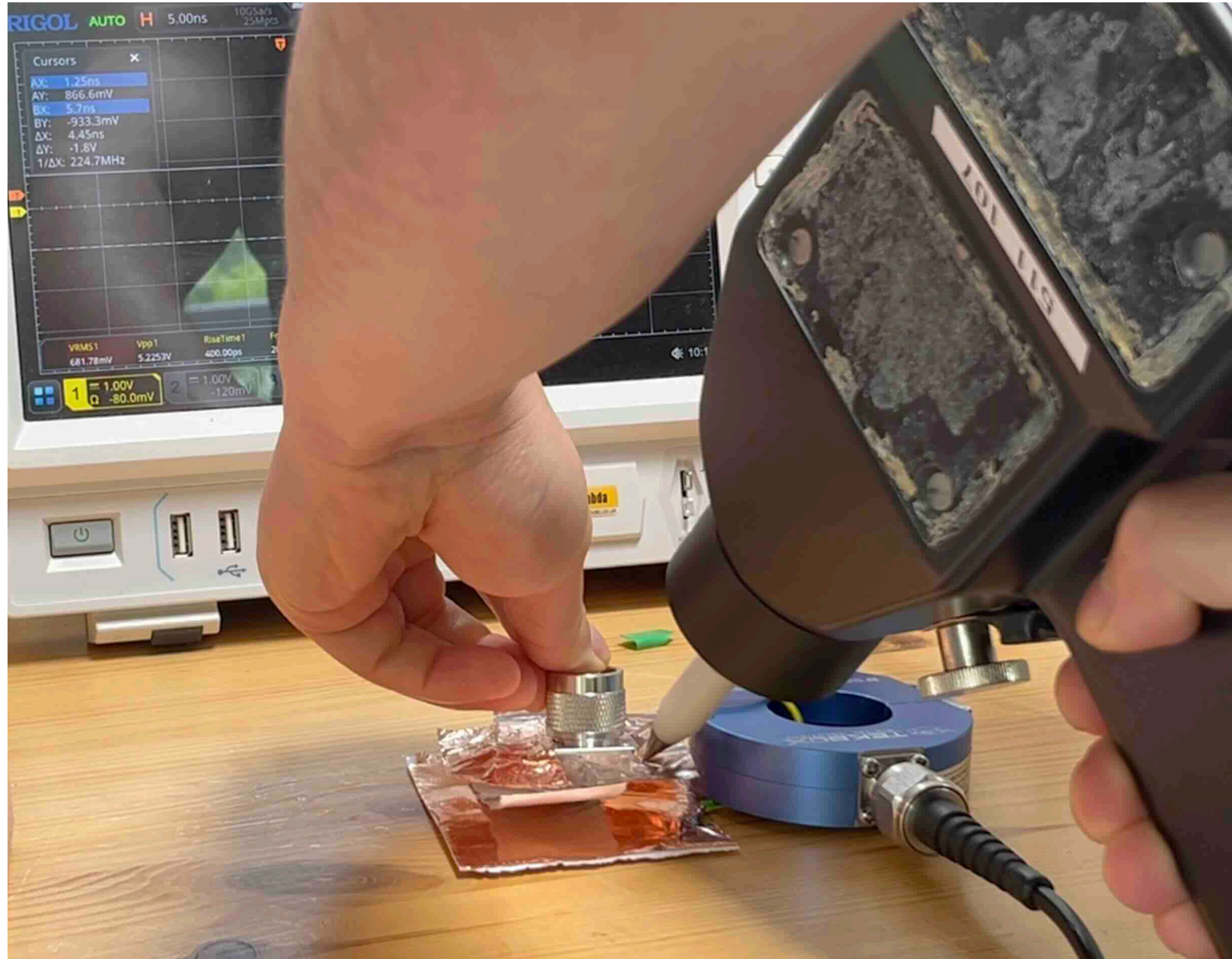
Resonance Circuits



The impedance curve of an L-C resonant circuit



Issues with a resonance structure



Resonance

Demonstration from an immunity point of view

Question 1

Interference between an AM car radio and an overhead power line is likely due to

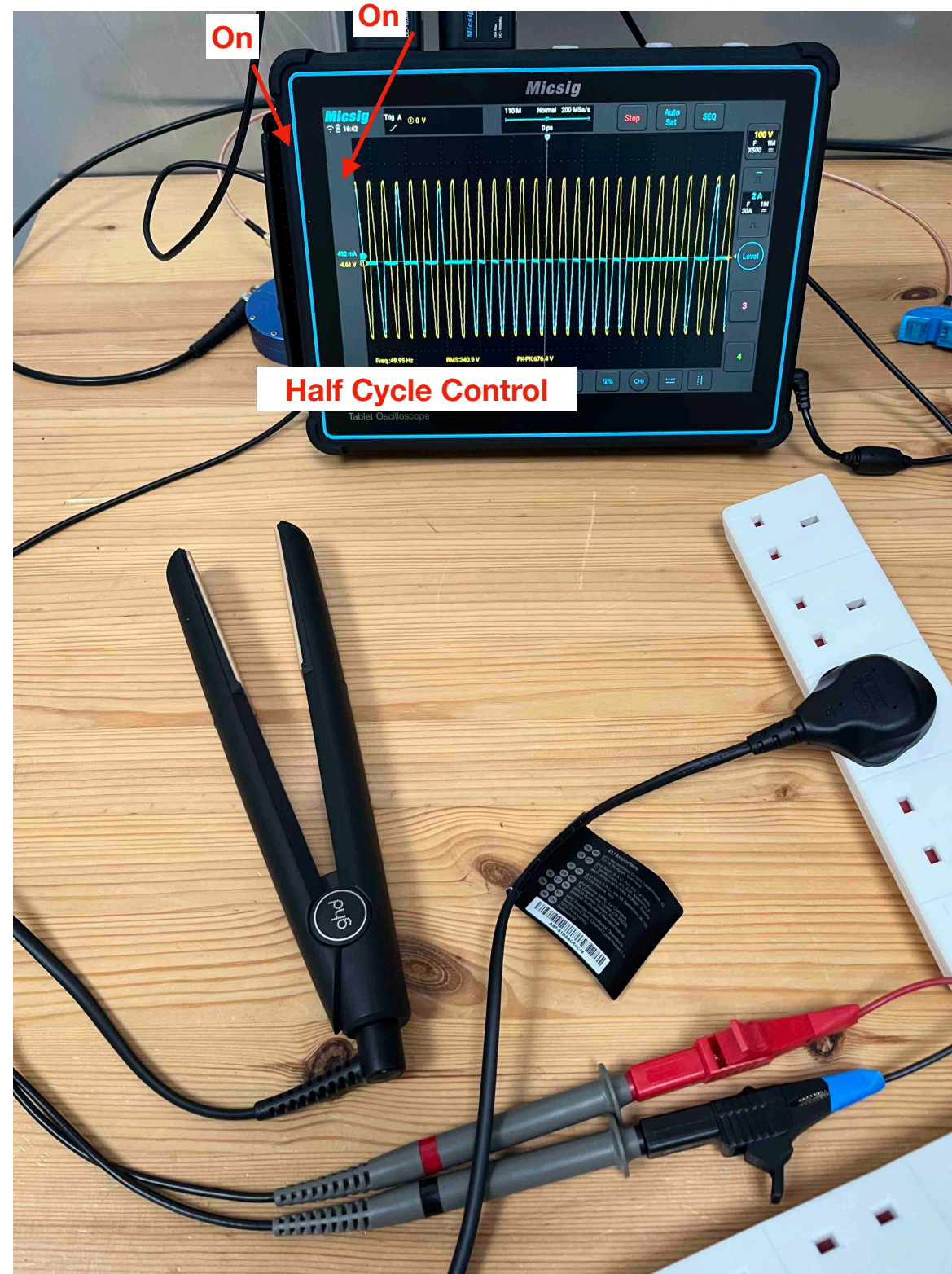
- A. Conducted coupling
- B. E-field coupling
- C. Magnetic field coupling
- D. Radiation coupling



Fundamentals - Module 2

Suited for advanced level design engineers.

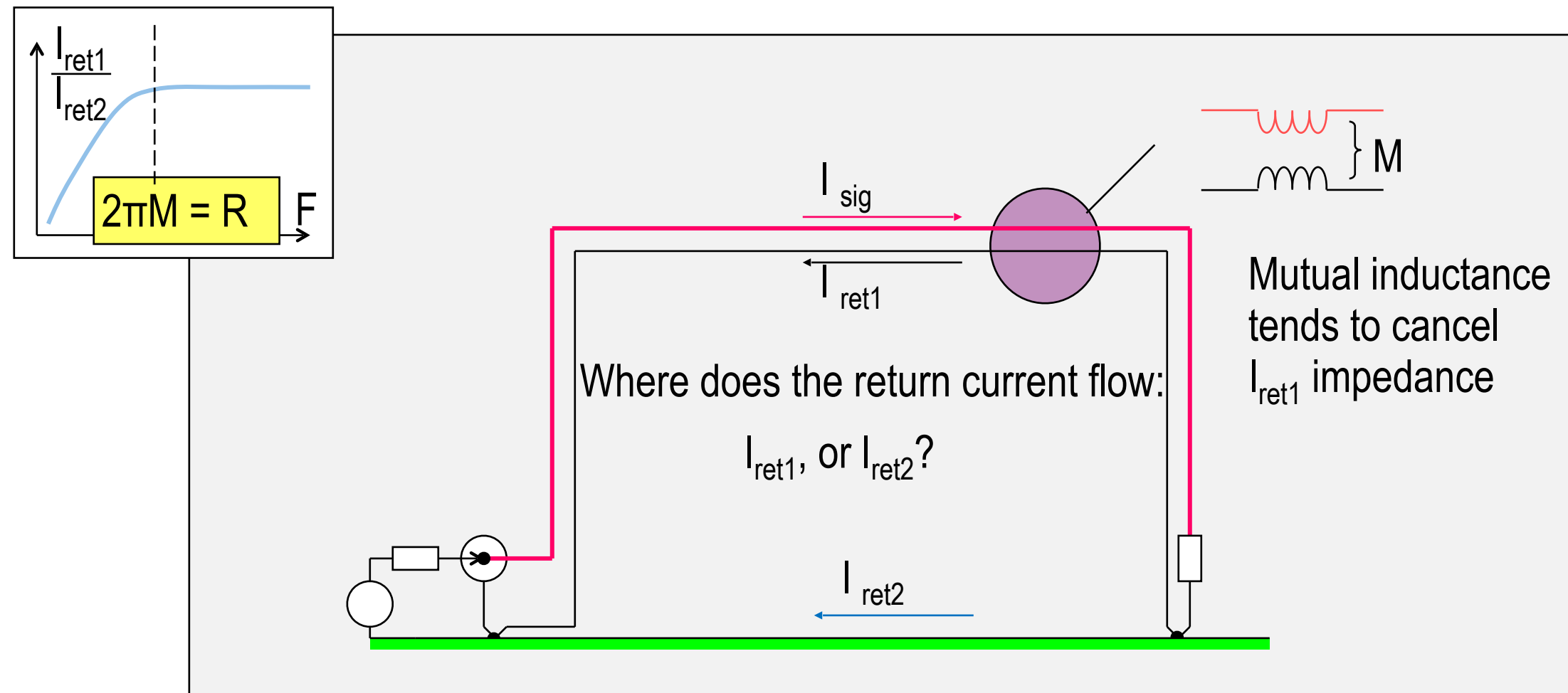
Seeing is believing; with time-domain demonstrations, engineers will grasp the concepts introduced in this module. Real-life case studies also help engineers to understand the EMC tests better.



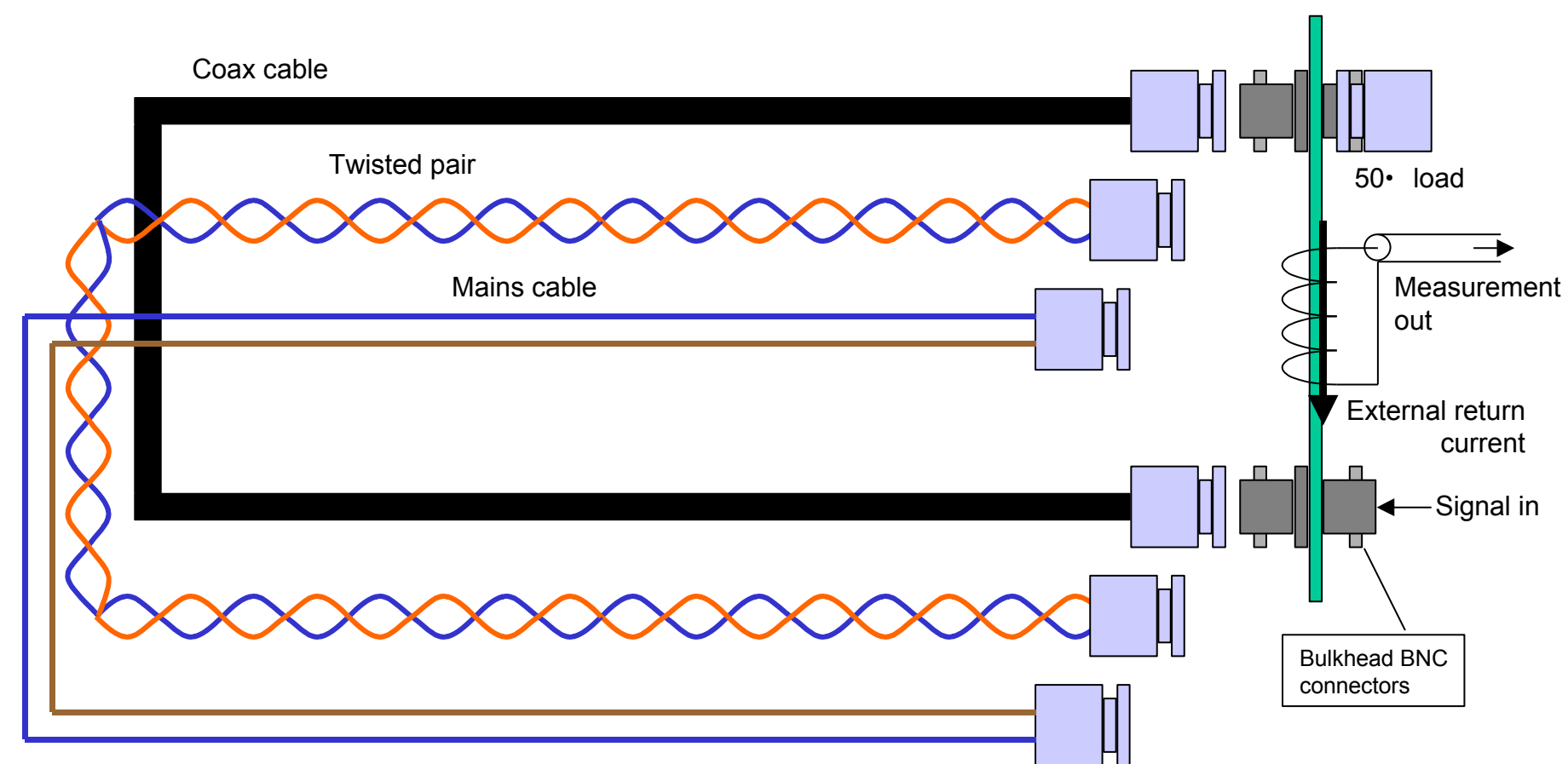
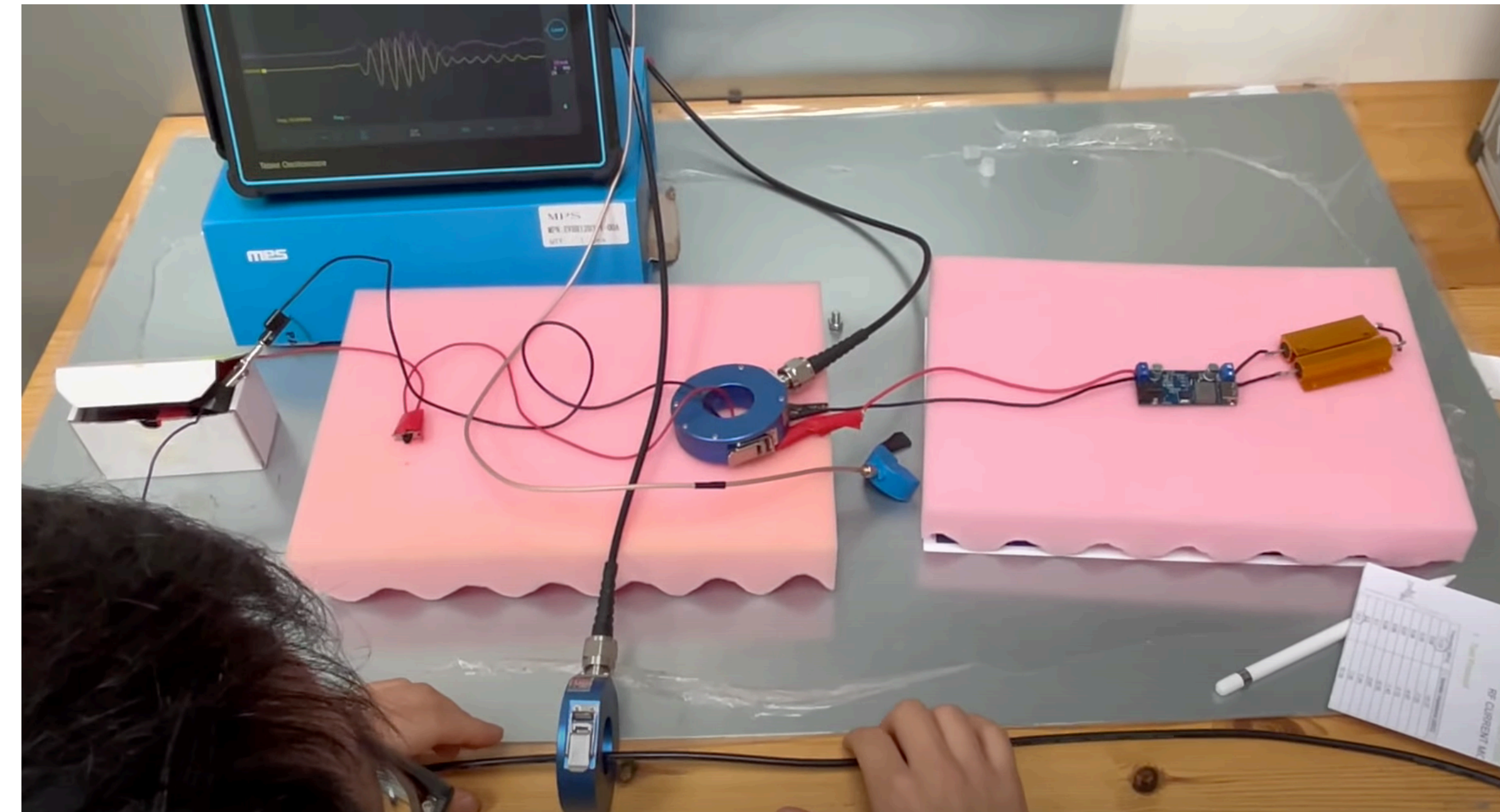
- Low vs. High Frequency with a Demonstration - Reinforcing the Concept of Loop Area and Inductance
- Differential Versus Common-Mode Noise with a Demonstration - Understanding Common-Mode Noise Is Essential for Solving EMI Issues
- Resonance Structure
- The Science Behind EMC Tests (A Walkthrough of Common EMC Tests) - Engineers Should Understand the Why and How of EMC Tests Before They Begin Designing a Compliance Product
- Pitfalls of EMC Tests through Real Life Case Studies

Demonstrations

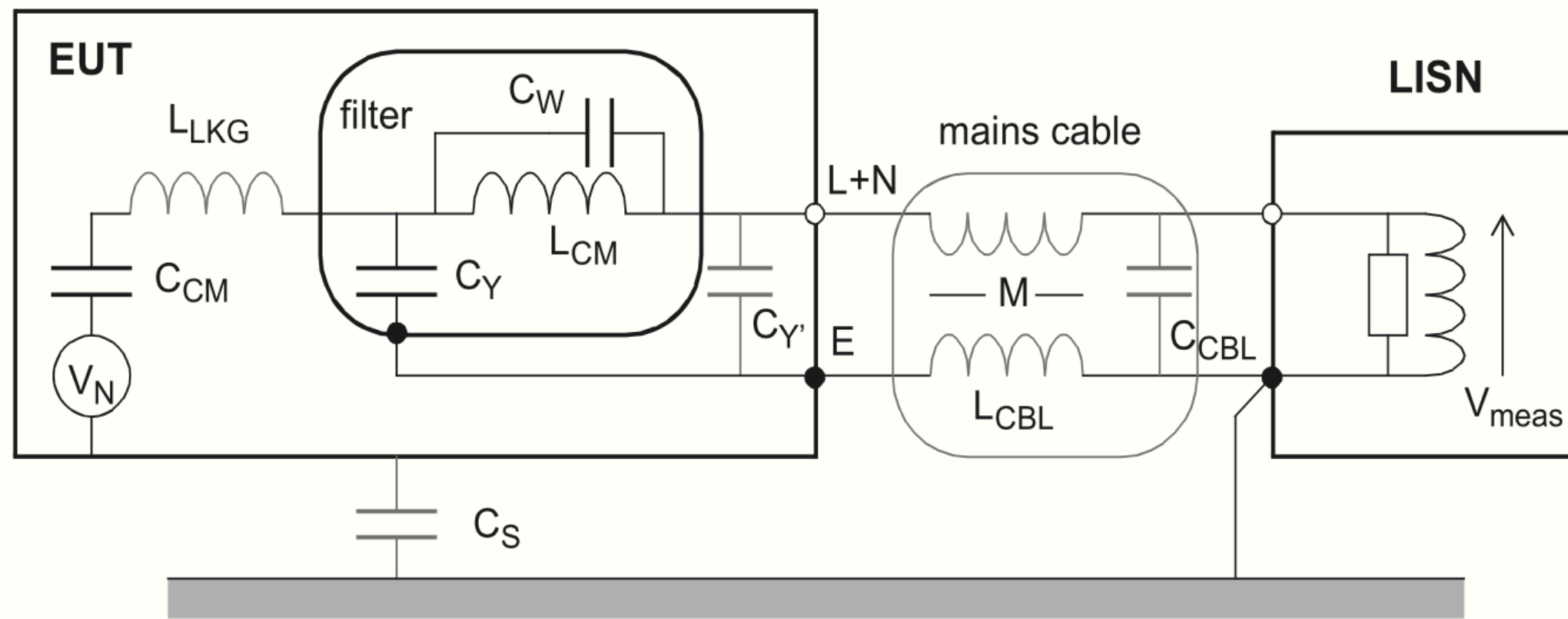
The ground return path demo



DM vs CM demo



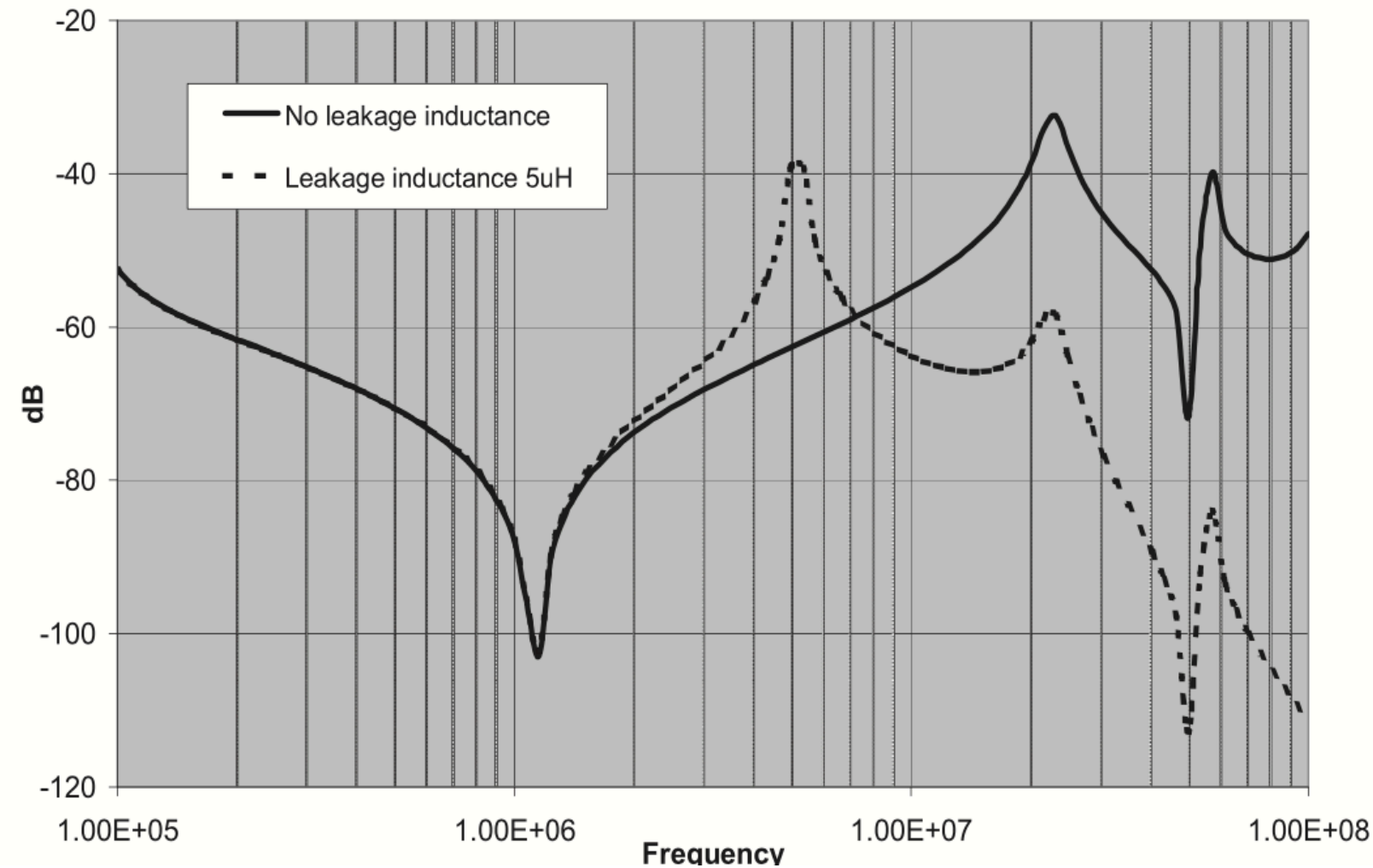
A Walkthrough of EMC Tests



(a) equivalent circuit in common mode

(b) model results
(attenuation $V_N - V_{meas}$)

$C_{CM} = 200\text{pF}$
 $C_Y = 4400\text{pF}$
 $L_{CM} = 1\text{mH}$
 $C_W = 20\text{pF}$
 $C_S = 5\text{pF}$
 $L_{CBL} = 2\mu\text{H}$
 $M = 0.7$
 $C_{CBL} = 20\text{pF}$
 Dotted line:
 $L_{LKG} = 5\mu\text{H}$



1 PK
VIEW

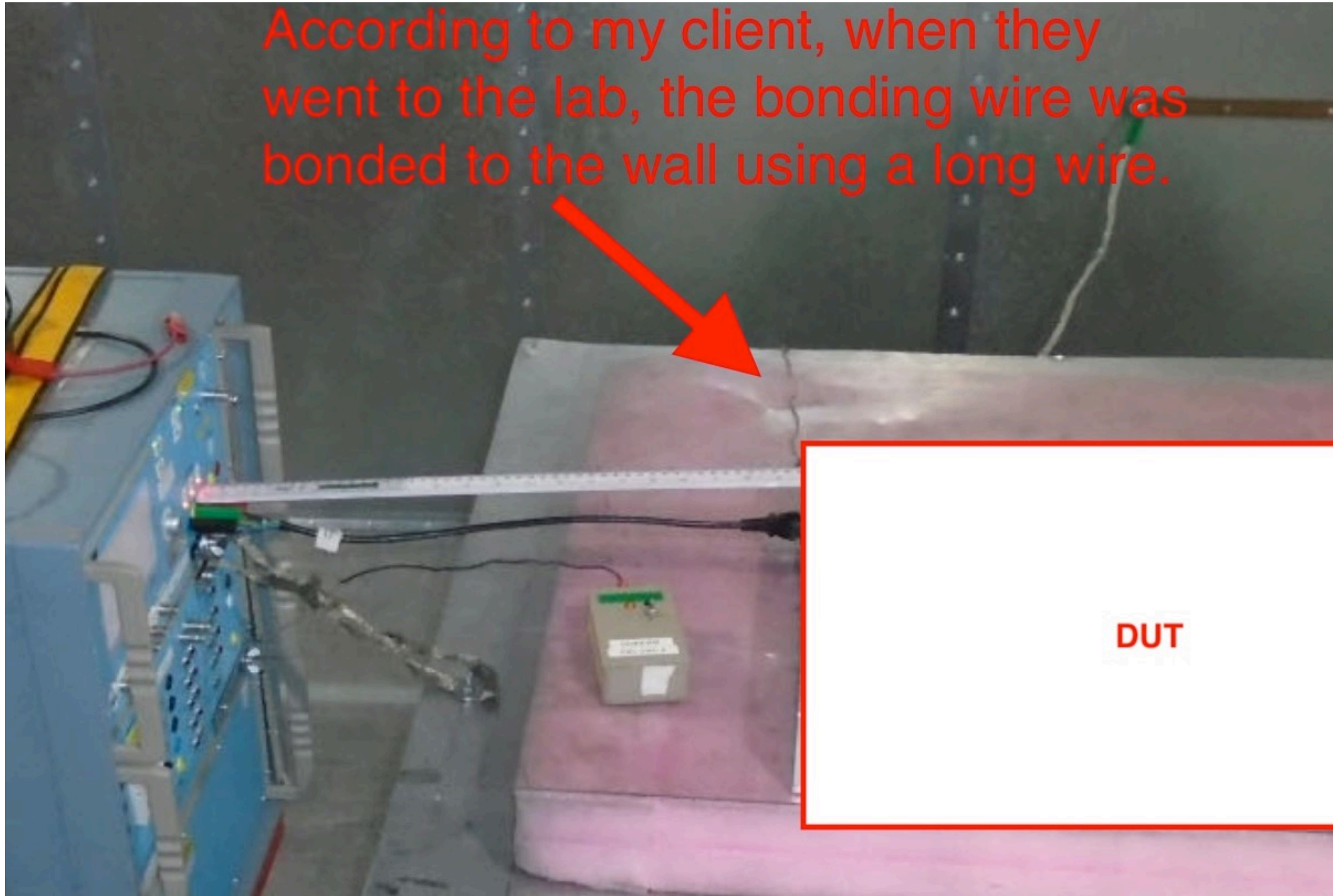


Center 2.121320344 MHz

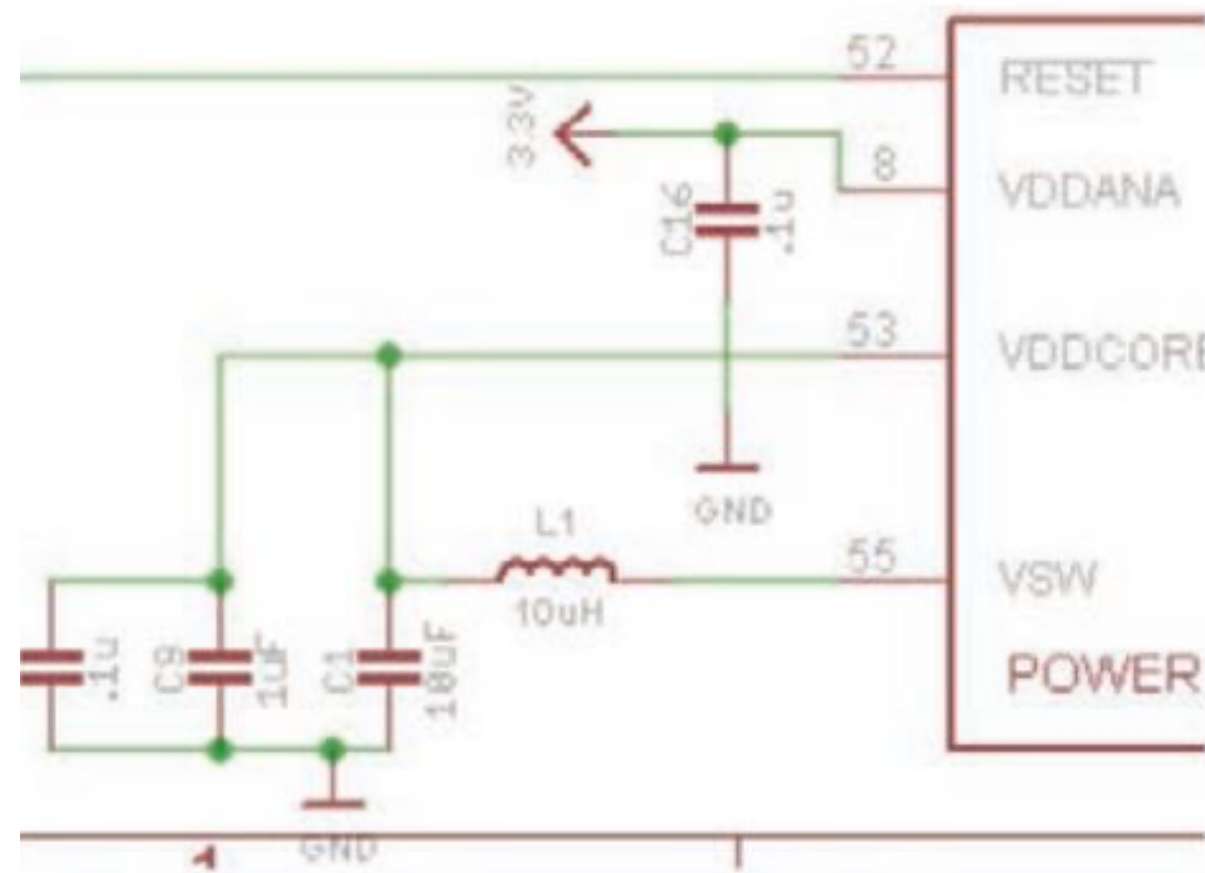
Span 29.85 MHz

Case Study 1

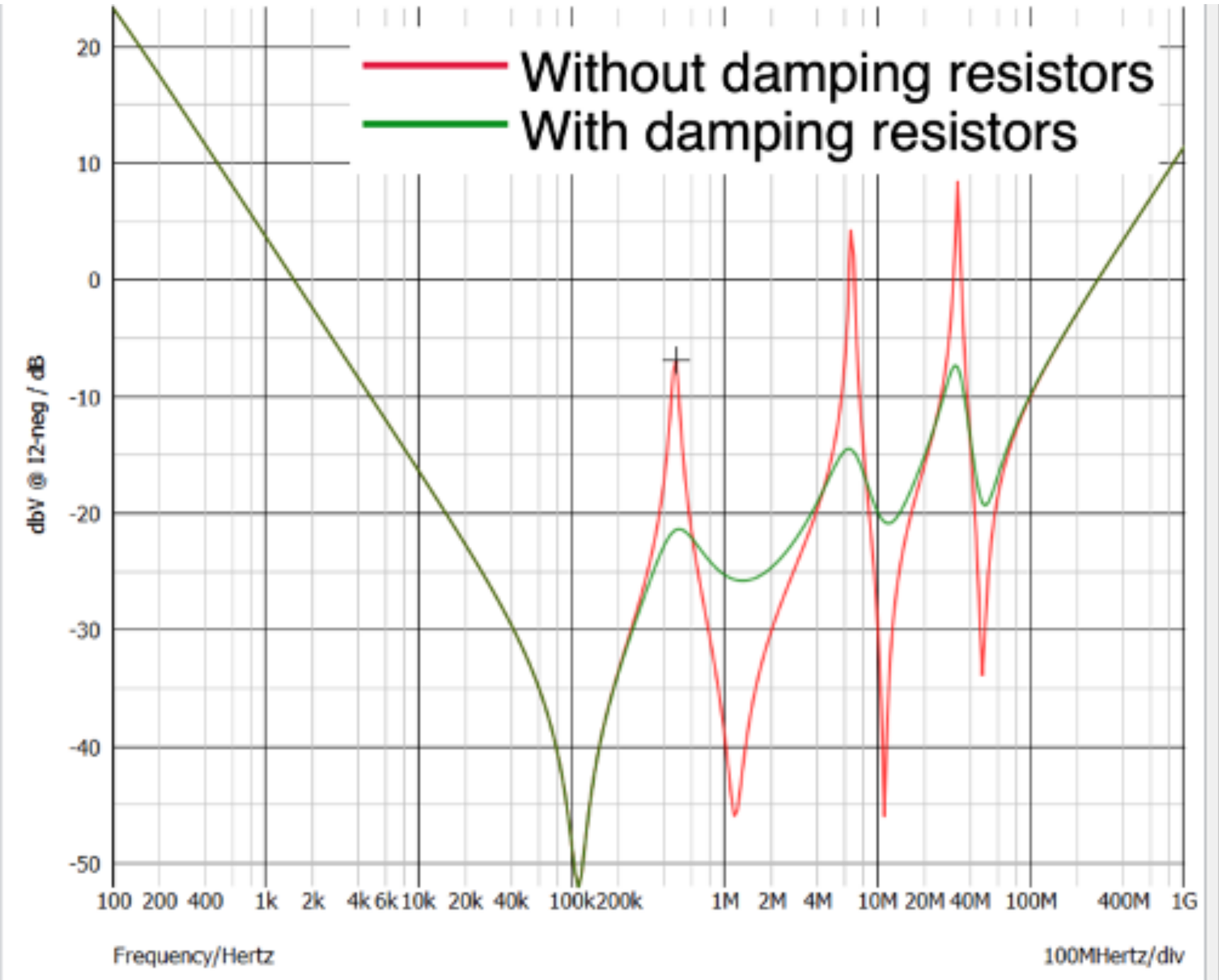
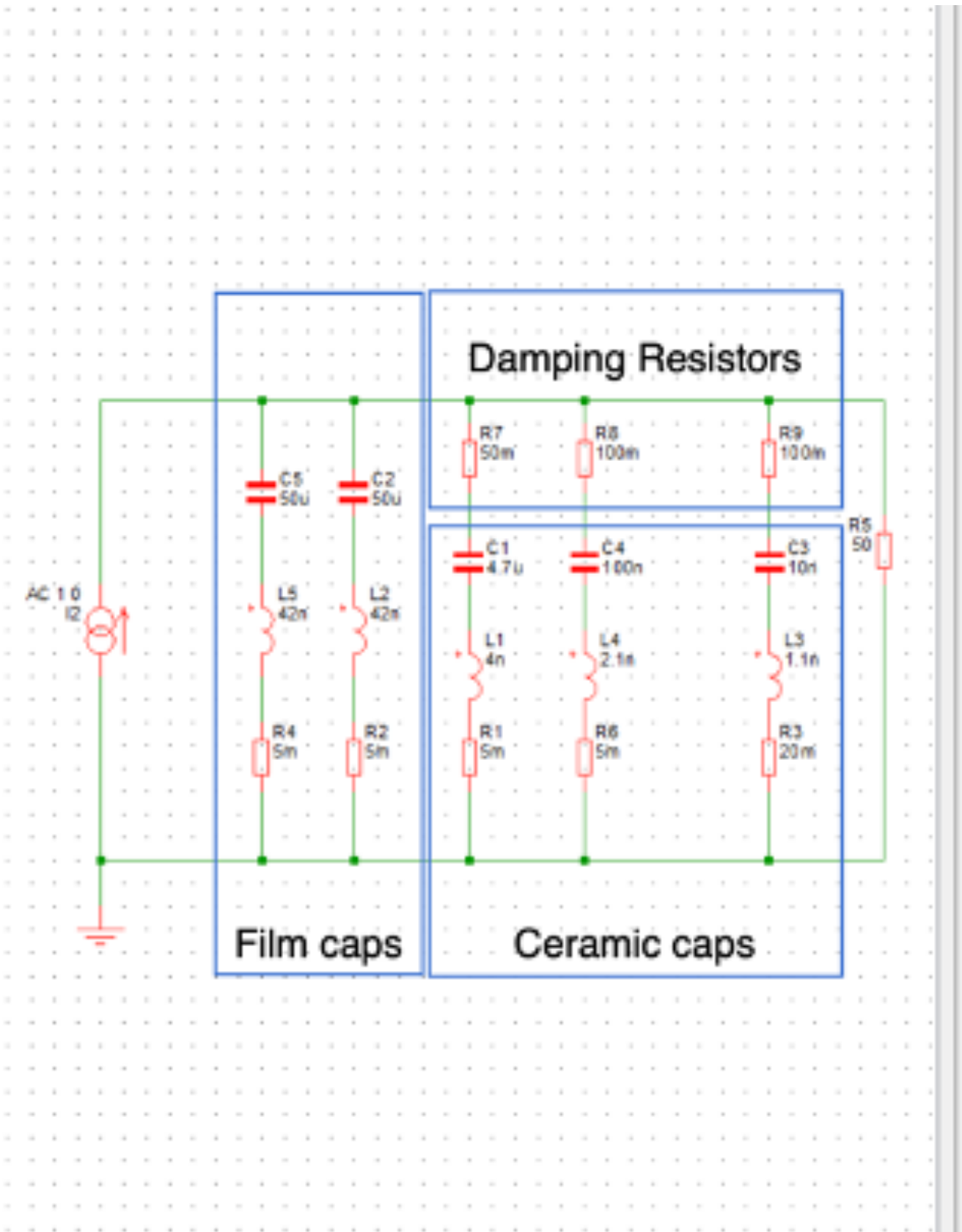
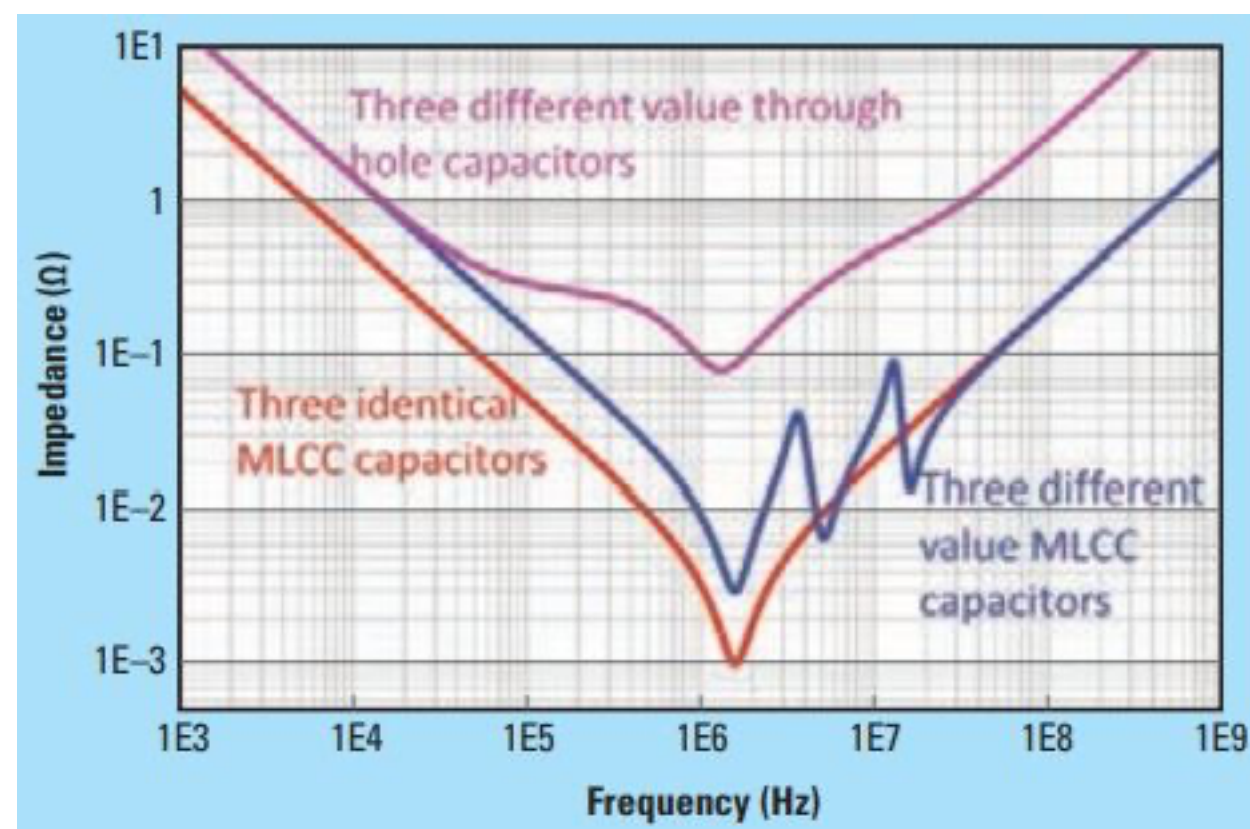
According to my client, when they went to the lab, the bonding wire was bonded to the wall using a long wire.



The Myth of Three Capacitor Values



0.1uF, 1uF and 10uF decoupling caps

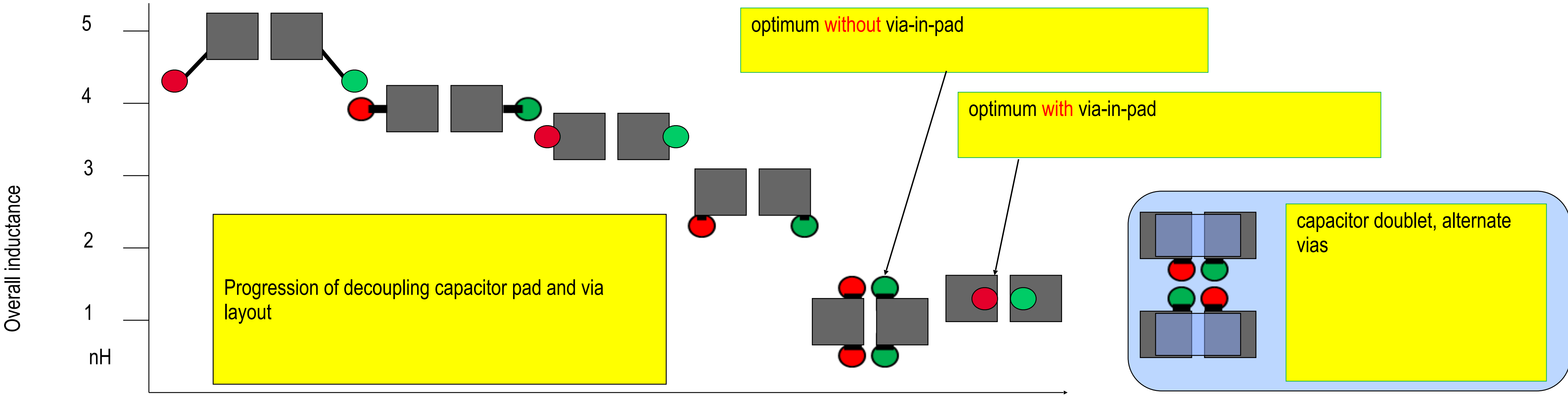


Resonance caused by multiple MLCCs could be a problem

Three capacitor values all the same large value may provide lower impedance across the spectrum than three different value capacitors (and without the parallel resonant peaks at intermediate frequencies), but this does not mean it is a more robust solution.

SMD capacitor layout

- The positioning of vias to power planes relative to SM pads affects the overall inductance of each instance of decoupling capacitor
 - lowest inductance is achieved with the + and - vias very close together (to benefit from mutual coupling)



Analog Susceptibility

